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1   Techniques for obtaining high performance in Java programs   88%

Iffat H. Kazi , Howard H. Chen , Berdenia Stanley , David J. Lilja
ACM Computing Surveys (CSUR) September 2000
Volume 32 Issue 3

> This survey describes research directions in techniques to improve the performance of programs written in the Java programming language. The standard technique for Java execution is interpretation, which provides for extensive portability of programs. A Java interpreter dynamically executes Java bytecodes, which comprise the instruction set of the Java Virtual Machine (JVM). Execution time performance of Java programs can be improved through compilation, possibly at the expense of portabili ...

2   A brief history of just-in-time   87%

John Aycock
ACM Computing Surveys (CSUR) June 2003
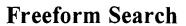Volume 35 Issue 2

> Software systems have been using "just-in-time" compilation (JIT) techniques since the 1960s. Broadly, JIT compilation includes any translation performed dynamically, after a program has started execution. We examine the motivation behind JIT compilation and constraints imposed on JIT compilation systems, and present a classification scheme for such systems. This classification emerges as we survey forty years of JIT work, from 1960--2000.

3   Efficient Java exception handling in just-in-time compilation   85%

Seungll Lee , Byung-Sun Yang , Suhyun Kim , Seongbae Park , Soo-Mook Moon , Kemal Ebcioğlu , Erik Altman
Pr ceedings f the ACM 2000 c nference n Java Grande June 2000

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L23	l4 and (rever$ or oppos$)	0	L23
L22	l4 and (memory$ or data or cache$)	1	L22
L21	l4 and execut$	1	L21
L20	l4 and (load$ OR STOR$)	1	L20
L19	l4 and load$ OR STOR$	1083749	L19
L18	l4 and (except$ or error$ or signal$)	0	L18
L17	l4 and float$	0	L17
L16	l4 and double	0	L16
L15	l4 and swap$	0	L15
L14	l4 and (operand or depth$ or stack$)	1	L14
L13	(sipush or bipush) and (overflow$ or underflow$)	17	L13
L12	(sipush or bipush) same (overflow$ or underflow$)	0	L12
L11	(sipush or bipush) near5 (overflow$ or underflow$)	0	L11
L10	l1 and sipush and bipush	0	L10

L9	l4 and (overflow$ or underflow$)	0	L9
L8	l4 and overflow$ and underflow$	0	L8

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L7	l4 and overflow$ and underflow$	0	L7

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L6	l4 and overflow$ and underflow$	0	L6
L5	l1 and overflow$ and underflow$	1	L5

DB=USPT; PLUR=YES; OP=ADJ

L4	5875336.pn.	1	L4
L3	l1 and execut$	1	L3
L2	L1 and (execut$ near5 stack$)	1	L2
L1	6332215.pn.	1	L1

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1 **Techniques for obtaining high performance in Java programs**   99%
Iffat H. Kazi , Howard H. Chen , Berdenia Stanley , David J. Lilja
ACM Computing Surveys (CSUR) September 2000
Volume 32 Issue 3
> This survey describes research directions in techniques to improve the performance of programs written in the Java programming language. The standard technique for Java execution is interpretation, which provides for extensive portability of programs. A Java interpreter dynamically executes Java bytecodes, which comprise the instruction set of the Java Virtual Machine (JVM). Execution time performance of Java programs can be improved through compilation, possibly at the expense of portabili ...

2 **Improving Java performance using hardware translation**   94%
Ramesh Radhakrishnan , Ravi Bhargava , Lizy K. John
Proceedings of the 15th international conference on Supercomputing June 2001

> State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

3 **LLVA: A Low-level Virtual Instruction Set Architecture**   92%
Vikram Adve , Chris Lattner , Michael Brukman , Anand Shukla , Brian Gaeke
Pr ceedings f the 36th Annual IEEE/ACM Internati nal Symp sium n Micr architecture December 2003
> A virtual instruction set architecture (V-ISA) implementedvia a processor-specific

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processor and stack and instruction and register and   Search

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1 **Early load address resolution via register tracking**
Bekeman, M.; Yoaz, A.; Gabbay, F.; Jourdan, S.; Kalaev, M.; Ronen, R.;
Computer Architecture, 2000. Proceedings of the 27th International Symposiu
on , 10-14 June 2000
Pages:306 - 315

[Abstract]   [PDF Full-Text (964 KB)]   **IEEE CNF**

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2 **An X86 microprocessor with multimedia extensions**
Draper, D.A.; Crowley, M.P.; Holst, J.; Favor, G.; Schoy, A.; Ben-Meir, A.; Tru Khanna, R.; Wendell, D.; Krishna, R.; Nolan, J.; Partovi, H.; Johnson, M.; Lee Mallick, D.; Frydel, G.; Vuong, A.; Yu, S.; Maley, R.; Kauffmann, B.;
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC 1997 IEEE International , 6-8 Feb. 1997
Pages:172 - 173, 450

[Abstract]   [PDF Full-Text (872 KB)]   **IEEE CNF**

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Terms	Documents
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L12	717/146,147,148,149.ccls.	411	L12
L11	717/136,137,138,139,140.ccls.	494	L11
	DB=TDBD; PLUR=YES; OP=ADJ		
L10	L8	0	L10
	DB=DWPI; PLUR=YES; OP=ADJ		
L9	L8	0	L9
	DB=JPAB; PLUR=YES; OP=ADJ		
L8	cpu and (register$ near4 instruction$) and (stack$ near5 instruction$) and (translat$ or decod$ or compil$)and overflow$ and underflow$	0	L8
	DB=EPAB; PLUR=YES; OP=ADJ		
L7	cpu and (register$ near4 instruction$) and (stack$ near5 instruction$) and (translat$ or decod$ or compil$)and overflow$ and underflow$	0	L7

DB=USOC; PLUR=YES; OP=ADJ

<u>L6</u>	cpu and (register$ near4 instruction$) and (stack$ near5 instruction$) and (translat$ or decod$ or compil$)and overflow$ and underflow$	2	<u>L6</u>

DB=PGPB; PLUR=YES; OP=ADJ

<u>L5</u>	cpu and (register$ near4 instruction$) and (stack$ near5 instruction$) and (translat$ or decod$ or compil$)and overflow$ and underflow$	14	<u>L5</u>

DB=USPT; PLUR=YES; OP=ADJ

<u>L4</u>	L3 and java	17	<u>L4</u>
<u>L3</u>	L2 and exception$	162	<u>L3</u>
<u>L2</u>	L1 and overflow$ and underflow$	204	<u>L2</u>
<u>L1</u>	cpu and (register$ near4 instruction$) and (stack$ near5 instruction$) and (translat$ or decod$ or compil$)	941	<u>L1</u>

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